WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a wiring substrate having a main surface, a back surface, a plurality of connection terminals provided on said main surface and a plurality of external electrodes provided on said back surface;

a first semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said first semiconductor chip and a plurality of electrodes created on said main surface of said first semiconductor chip;

a second semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said second semiconductor chip and a plurality of electrodes created on said main surface of said second semiconductor chip; and

a resin sealing body formed on said main surface of said wiring substrate and used for sealing said first semiconductor chip and said second semiconductor chip; and

a plurality of wires for connecting said electrodes provided on said second semiconductor chip to said respective connection terminals provided on said wiring substrate,

wherein said first semiconductor chip is placed with said main surface of said first semiconductor chip interfacing with said main surface of said wiring substrate in such a way that

said electrodes provided on said main surface of said first semiconductor chip interface with said respective electrodes provided on said main surface of said wiring substrate, and

wherein said second semiconductor chip is placed above said main surface of said wiring substrate, sandwiching said first semiconductor chip in conjunction with said wiring substrate.

2. A semiconductor device according to claim 1, wherein said first and second semiconductor chips are placed above said main surface of said wiring substrate in such a way that said back surface of said first semiconductor chip interfaces with said back surface of said second semiconductor chip through an adhesive.

3. A semiconductor device according to claim 2, said semiconductor device having a plurality of wires for electrically connecting said electrodes provided on said second semiconductor chip to said respective electrodes provided on said wiring substrate.

4. A semiconductor device according to claim 3, wherein said electrodes provided on said first semiconductor chip are welded with said respective electrodes provided on said wiring substrate in a pressure welding process.

5. A semiconductor device according to claim 4, wherein said main surface of said first semiconductor chip is fixed on said main surface of said wiring substrate through an adhesive between said main surfaces.

6. A semiconductor device according to claim 1, wherein a bus frequency of said first semiconductor chip is higher than a bus frequency of said second semiconductor chip.

7. A semiconductor device according to claim 6 wherein said first semiconductor chip is a logic chip and said second semiconductor chip is a memory chip.

8. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a wiring substrate having a plurality of electrodes created on a main surface thereof;

(b) preparing a first semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface of said first semiconductor chip and a plurality of electrodes created on said main surface of said first semiconductor chip;

(c) preparing a second semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices

created on said main surface of said second semiconductor chip and a plurality of electrodes created on said main surface of said second semiconductor chip and having a thickness smaller than a thickness of said first semiconductor chip;

(d) placing said first semiconductor chip on said main surface of said wiring substrate with said main surface of said first semiconductor chip interfacing with said main surface of said wiring substrate in such a way that said electrodes provided on said main surface of said first semiconductor chip interface with said respective electrodes provided on said main surface of said wiring substrate;

(e) after said step (d), applying a pressure to said back surface of said first semiconductor chip to electrically connect said electrodes provided on said first semiconductor chip to said respective electrodes provided on said wiring substrate;

(f) after said step (e), placing said second semiconductor chip on said back surface of said first semiconductor chip so as to make said back surface of said second semiconductor chip interface with said back surface of said first semiconductor chip through an adhesive by applying a pressure smaller than said pressure applied in said step (e);

(g) electrically connecting said electrodes created on said second semiconductor chip to said respective electrodes provided on said wiring substrate by using a plurality of wires;

and

(h) forming a resin sealing body for sealing said first semiconductor chip, said second semiconductor chip and said wires.

9. A semiconductor device manufacturing method according to claim 8, wherein in said step (e), heat is applied to said first semiconductor chip at the same time as said applied pressure.

10. A semiconductor device manufacturing method according to claim 9, wherein said heat applied in said step (e) hardens the thermally-hardening resin placed between said main surface of said first semiconductor chip and said main surface of said wiring substrate, fixing said first semiconductor chip on said main surface of said wiring substrate through said the thermally hardening resin.

11. A semiconductor device manufacturing method according to claim 8, wherein in said step (e), a supersonic wave is radiated to said first semiconductor chip at the same time as said applied pressure.

12. A semiconductor device manufacturing method according to claim 11, wherein a metallic bump to serve as a protruding electrode is created on each of said electrodes provided on said

first semiconductor chip and, in said step (e), a supersonic wave is radiated to said first semiconductor chip at the same time as said applied pressure so as to take said first semiconductor chip into contact with said wiring substrate through ultrasonic metal-to-metal connection.

13. A semiconductor device manufacturing method according to claim 8, wherein said electrodes provided on said first semiconductor chip each comprise a pad created on said main surface of said first semiconductor chip and a protruding electrode placed on said pad.

14. A semiconductor device manufacturing method according to claim 8, further comprising, after said step (h), the step of creating a plurality of protruding electrodes created on a back surface of said wiring substrate, which are each used as an external electrode connected to a corresponding one of said electrodes provided on said main surface of said wiring surface.

15. A semiconductor device manufacturing method according to claim 8, further comprising, between said steps (e) and (f), the steps of:

(i) preparing a third semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface and a plurality of electrodes

created on said main surface;

(j) placing said third semiconductor chip on said main surface of said wiring substrate with said main surface of said third semiconductor chip interfacing with said main surface of said wiring substrate in such a way that said electrodes provided on said main surface of said third semiconductor chip interface with said respective electrodes provided on said main surface of said wiring substrate; and

(k) after said step (j), applying a pressure to said back surface of said third semiconductor chip to electrically connect said electrodes provided on said third semiconductor chip to said respective electrodes provided on said wiring substrate.

16. A semiconductor device manufacturing method according to claim 15, further comprising, after said step (k), the steps of:

(l) preparing a fourth semiconductor chip having a main surface, a back surface, a plurality of semiconductor devices created on said main surface and a plurality of electrodes created on said main surface and having a thickness smaller than a thickness of said third semiconductor chip;

(m) placing said fourth semiconductor chip on said back surface of said third semiconductor chip so as to make said back surface of said fourth semiconductor chip interface with said

back surface of said third semiconductor chip through an adhesive by applying a pressure smaller than said pressure applied in said step (k); and

(n) electrically connecting said electrodes created on said fourth semiconductor chip to said respective electrodes provided on said wiring substrate by using a plurality of wires.

17. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces and provided with a resin injection entrance created on said first side surface;

(b) preparing a wiring substrate having a main surface, preparing a first semiconductor chip fixed on said main surface of said wiring substrate and preparing a second semiconductor chip fixed on said first semiconductor chip;

(c) placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c) injecting resin through said resin injection entrance in order to seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said

first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, the length of said first semiconductor chip exceeds the length of said second semiconductor chip.

18. A semiconductor device manufacturing method according to claim 17 wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said first side surface of said cavity, the length of said first semiconductor chip is smaller than the length of said second semiconductor chip.

19. A semiconductor device manufacturing method according to claim 17, wherein said mold has an air hole created on said second side surface of said cavity.

20. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces and provided with a plurality of resin injection entrances created on said first side surface;

(b) preparing a wiring substrate having a main surface and a plurality of device areas created thereon, preparing a first semiconductor chip fixed on each of said device areas of said wiring substrate and preparing a second semiconductor chip fixed on each of said first semiconductor chips;

(c) placing said wiring substrate, said first semiconductor chips and said second semiconductor chips inside said cavity, and then collectively cover said device areas by using said cavity; and

after said step (c), injecting resin through said resin injection entrances associated with said device areas in order to collectively seal and hold said first and second semiconductor chips,

wherein in said step (c), said wiring substrate, said first semiconductor chip and said second semiconductor chip are arranged in such a way that, on a cross section parallel to said third side surface of said cavity, said length of each of said first semiconductor chips exceeds said length of said second semiconductor chip stacked on said first semiconductor chip.

21. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first

and second side surfaces and provided with a resin injection entrance created on said first side surface;

(b) preparing a wiring substrate having a main surface, preparing a first semiconductor chip fixed on said main surface of said wiring substrate through an adhesive and preparing a second semiconductor chip fixed on said first semiconductor chip;

(c) placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c), injecting resin through said resin injection entrance in order to seal and hold said first and second semiconductor chips,

wherein in said step (b), said adhesive is used to fill up a space between said main surface of said wiring substrate and said second semiconductor chip's portion protruding in horizontal-surface directions out from a periphery of said first semiconductor chip.

22. A semiconductor device manufacturing method according to claim 21, wherein in said step (d), a pressure is applied to said resin when said resin is injected.

23. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a mold provided with a cavity having first and second side surfaces facing each other and third and fourth surfaces facing each other and coming in contact with said first and second side surfaces and provided with a resin injection entrance created on said first side surface;

(b) preparing a wiring substrate having a main surface, preparing a first semiconductor chip fixed on said main surface of said wiring substrate through an adhesive and preparing a second semiconductor chip fixed on said first semiconductor chip;

(c) placing said wiring substrate, said first semiconductor chip and said second semiconductor chip inside said cavity; and

(d) after said step (c), injecting resin through said resin injection entrance in order to seal and hold said first and second semiconductor chips,

wherein in said step (b), said adhesive is used to fill up a space between said main surface of said wiring substrate and said second semiconductor chip's portion protruding in a direction to said second side surface of said cavity out from a periphery of said first semiconductor chip.

24. A semiconductor device manufacturing method according to claim 23 wherein in said step (d), a pressure is applied to said resin when said resin is injected.

25. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a wiring substrate having a main surface, a plurality of first electrodes created on said main surface and a plurality of second electrodes created on said main surface;

(b) preparing a first semiconductor-chip group comprising a plurality of semiconductor chips each having a main surface, a plurality of protruding electrodes provided on said main surface and a plurality of semiconductor devices created on said main surface and preparing a second semiconductor-chip group comprising a plurality of semiconductor chips each having a main surface, a plurality of protruding electrodes provided on said main surface and a plurality of semiconductor devices created on said main surface;

(c) placing a first adhesive on each of said first electrodes created on said wiring substrate;

(d) after said step (c), thermally crimping said semiconductor chips pertaining to said first semiconductor-chip group in order to fix said semiconductor chips pertaining to said first semiconductor-chip group on said main surface of said wiring substrate through said first adhesive and in order to electrically connect said protruding electrodes provided on each of said semiconductor chips pertaining to said first

semiconductor-chip group to said respective first electrodes provided on said wiring substrate;

(e) after said step (c), placing a second adhesive on each of said second electrodes created on said wiring substrate; and

(f) after said step (e), thermally crimping said semiconductor chips pertaining to said second semiconductor-chip group in order to fix said semiconductor chips pertaining to said second semiconductor-chip group on said main surface of said wiring substrate through said second adhesive and in order to electrically connect said protruding electrodes provided on each of said semiconductor chips pertaining to second first semiconductor-chip group to said respective second electrodes provided on said wiring substrate.

26. A semiconductor device manufacturing method according to claim 25, wherein said first adhesive placed in said step (c) comprises first and second portions put on said main surface of said wiring substrate and separated from each other and,

wherein in said step (e), said second adhesive is provided between said first and second portions of said first adhesive.

27. A semiconductor device manufacturing method according to claim 25,

wherein pieces of said first adhesive placed in said step (c) are laid out to form a staggered array, and

wherein pieces of said second adhesive placed in said step (e) are laid out to form a staggered array with each piece of said second adhesive located at a position adjacent to one of said pieces of said first adhesive.

28. A semiconductor device manufacturing method according to claim 25, wherein said first and second adhesives are each thermally hardening resin: in said stop (d), said first adhesive is thermally hardened, and in said stop (f), said second adhesive is thermally hardened.

29. A semiconductor device manufacturing method according to claim 25, wherein said first and second adhesives are each a film made of thermally hardening resin.

30. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a wiring substrate having a main surface and a plurality of electrodes created on said main surface;

(b) preparing a first semiconductor chip having a main surface, a plurality of electrodes created on said main surface and a plurality of semiconductor devices created on said main surface;

(c) placing said first semiconductor chip on said main surface of said wiring substrate separated by a first adhesive

from said first semiconductor chip;

(d) putting said first adhesive in a heat-treatment process to thermally harden said first adhesive in order to fix said first semiconductor chip on said main surface of said wiring substrate through said first adhesive;

(e) preparing a second semiconductor chip having a main surface, a plurality of electrodes created on said main surface and a plurality of semiconductor devices created on said main surface;

(f) after said step (d), placing said second semiconductor chip on said first semiconductor chip separated by a second adhesive from said second semiconductor chip;

(g) putting said second adhesive in a heat-treatment process to thermally harden said second adhesive with said second semiconductor chip held by using fittings in order to fix said second semiconductor chip on said first semiconductor chip through said second adhesive; and

(h) after said step (g), separating said fittings from said second semiconductor chip.

31. A semiconductor device manufacturing method according to claim 30, further comprising, between said steps (d) and (f), the steps of:

(i) preparing a third semiconductor chip having a main surface, a plurality of electrodes created on said main surface

and a plurality of semiconductor devices created on said main surface;

(j) placing said third semiconductor chip on said main surface of said wiring substrate separated by a third adhesive from said third semiconductor chip; and

(k) putting said third adhesive in a heat-treatment process to thermally harden said third adhesive in order to fix said third semiconductor chip on said main surface of said wiring substrate through said third adhesive.

32. A semiconductor device manufacturing method according to claim 31, comprising, after said step (k),the steps of:

(l) preparing a fourth semiconductor chip having a main surface, a plurality of electrodes created on said main surface and a plurality of semiconductor devices created on said main surface;

(m) after said step (d) placing said fourth semiconductor chip on said third semiconductor chip separated by a fourth adhesive from said fourth semiconductor chip;

(n) putting said fourth adhesive in a heat-treatment process to thermally harden said fourth adhesive with said fourth semiconductor chip held by using fittings in order to fix said fourth semiconductor chip on said third semiconductor chip through said fourth adhesive; and

(o) after said step (g), separating said fittings from said fourth semiconductor chip.

33. A semiconductor device manufacturing method according to claim 30, wherein the temperature of said heat-treatment process carried out on said first adhesive in said step (d) is higher than the temperature of said heat-treatment process carried out on said second adhesive in said step (g).

34. A semiconductor device manufacturing method comprising the steps of:

(a) preparing a wiring substrate having a main surface and a plurality of electrodes created on said main surface;

(b) putting said substrate in a heat-treatment process at a temperature of at least 100 degrees Celsius;

(c) after said step (b), putting a semiconductor chip on said main surface of said substrate separated from said semiconductor chip by an adhesive; and

(d) putting said adhesive in a heat-treatment process to thermally harden said adhesive in order to fix said semiconductor chip on said main surface of said wiring substrate through said adhesive.

35. A semiconductor device manufacturing method for stacking a first semiconductor chip, a second semiconductor chip and a third semiconductor chip on a main surface of a wiring substrate, comprising the steps of:

preparing said wiring substrate having said main surface, a back surface on a side opposite to said main surface and a plurality of electrodes created on said main surface;

preparing said first semiconductor chip having a main surface and a plurality of protruding electrodes created on said main surface;

preparing said second semiconductor chip having a main surface and a plurality of electrodes created on said main surface;

preparing said third semiconductor chip having a main surface and a plurality of electrodes created on said main surface;

placing said first semiconductor chip on said main surface of said wiring substrate in such a way that said main surface of said first semiconductor chip interfaces with said main surface of said wiring substrate; placing said second semiconductor chip on a back surface of said first semiconductor chip in such a way that a back surface of said second semiconductor chip interfaces with said back surface of said first semiconductor chip; placing said third semiconductor chip on said main surface of said second semiconductor chip in such a way that a back surface of said third semiconductor chip interfaces with said main surface of said second semiconductor chip; electrically connecting said first semiconductor chip to said electrodes created on said wiring substrate through said

protruding electrodes; and bonding said main surface of said first semiconductor chip to said main surface of said wiring substrate by a using an adhesive put between said main surfaces;

after said step of placing said first, second and third semiconductor chips on said wiring substrate, electrically connecting said electrodes created on said second semiconductor chip to said respective electrodes created on said wiring substrate by wires; and

after said step of placing said first, second and third semiconductor chips on said wiring substrate, electrically connecting said electrodes created on said third semiconductor chip to said respective electrodes created on said wiring substrate by wires,

wherein in said step of placing said first, second and third semiconductor chips on said wiring substrate, said third semiconductor chip is placed on said main surface of said second semiconductor chip in such a way that said electrodes created on said third semiconductor chip are positioned at locations on the outer side of an area in which said first semiconductor chip is placed; and

wherein in said step of electrically connecting said electrodes created on said third semiconductor chip to said respective electrodes created on said wiring substrate, said wires are connected to said electrodes created on said third semiconductor chip with a portion of said adhesive placed

between a plurality of electrodes provided on said third semiconductor chip, which are positioned at locations on an outer side of said first semiconductor chip, and said main surface of said wiring substrate in such a way that a gap between said back surface of said third semiconductor chip and said adhesive is smaller than the thickness of said third semiconductor chip.

36. A semiconductor device manufacturing method according to claim 35, also used for creating:

said adhesive's first portion between said main surface of said first semiconductor chip and said main surface of said wiring substrate;

said adhesive's second portion between said second semiconductor chip's back surface in an outer side of an area in which said first semiconductor chip is created and said main surface of said wiring substrate; and

said adhesive's third portion between said third semiconductor chip's back surface in an outer side of an area in which said first semiconductor chip is located as well as an area in which said second semiconductor chip is located and said main surface of said wiring substrate.

37. A semiconductor device manufacturing method according to claim 36, wherein said second potion of said adhesive is created

to have a thickness greater than the thickness of said first portion of said adhesive and said third potion of said adhesive is created to have a thickness greater than said thickness of said second portion of said adhesive.

38. A semiconductor device manufacturing method according to claim 37, wherein said step of placing said first, second and third semiconductor chips on said wiring substrate comprises:

a step including the steps of:

thermally crimping said first semiconductor chip on said main surface of said wiring substrate by using thermal-crimp fittings in such a way that said main surface of said first semiconductor chip interfaces with said main surface of said wiring substrate as well as electrically connecting said first semiconductor chip to a plurality of electrodes provided on said wiring substrate through said protruding electrodes; and

bonding said main surface of said first semiconductor chip to said main surface of said wiring substrate by using an adhesive between said main surfaces;

after said step of placing said first semiconductor chip, bonding said second semiconductor chip to said first semiconductor chip in such a way that said back surface of said second semiconductor chip interfaces with said back surface of said first semiconductor chip; and

after said step of placing said second semiconductor chip,

bonding said third semiconductor chip to said second semiconductor chip in such a way that said back surface of said third semiconductor chip interfaces with said main surface of said second semiconductor chip.

39. A semiconductor device manufacturing method according to claim 38, wherein in said step of placing said first semiconductor chip, a protrusion of said thermal-crimp fittings is used for setting a difference in thickness between a second portion of said adhesive and a third portion of said adhesive.

40. A semiconductor device manufacturing method according to claim 38, wherein said adhesive includes thermally hardening resin.

41. A semiconductor device manufacturing method according to claim 37, wherein said step of placing said first, second and third semiconductor chips on said wiring substrate comprises the steps of:

bonding said second semiconductor chip to said back surface of said first semiconductor chip in such a way that said back surface of said second semiconductor chip interfaces with said back surface of said first semiconductor chip;

after said step of bonding said second semiconductor chip, placing said first semiconductor chip on said main surface of said wiring substrate by execution of the steps of: thermally

crimping said first semiconductor chip on said main surface of said wiring substrate by using thermal-crimp fittings in such a way that said main surface of said first semiconductor chip interfaces with said main surface of said wiring substrate as well as electrically connecting said first semiconductor chip to a plurality of electrodes provided on said wiring substrate through said protruding electrodes; and bonding said main surface of said first semiconductor chip to said main surface of said wiring substrate by using an adhesive put between said main surfaces;

after said step of placing said first semiconductor chip, bonding said third semiconductor chip to said main surface of said second semiconductor chip in such a way that said back surface of said third semiconductor chip interfaces with said main surface of said second semiconductor chip.

42. A semiconductor device manufacturing method according to claim 41, wherein said second semiconductor chip is bonded to said back surface of said first semiconductor chip through an adhesive including thermally hardening resin and said third semiconductor chip is bonded to said main surface of said second semiconductor chip through an adhesive including thermally hardening resin.

43. A semiconductor device manufacturing method for stacking

a first semiconductor chip, a second semiconductor chip and a third semiconductor chip on a main surface of a wiring substrate, comprising the steps of:

preparing said wiring substrate having said main surface, a back surface on a side opposite to said main surface and a plurality of electrodes created on said main surface;

preparing said first semiconductor chip having a main surface and a plurality of protruding electrodes created on said main surface;

preparing said second semiconductor chip having a main surface and a plurality of electrodes created on said main surface;

preparing said third semiconductor chip having a main surface and a plurality of electrodes created on said main surface;

placing said first semiconductor chip on said main surface of said wiring substrate in such a way that said main surface of said first semiconductor chip interfaces with said main surface of said wiring substrate; placing said second semiconductor chip on a back surface of said first semiconductor chip in such a way that a back surface of said second semiconductor chip interfaces with said back surface of said second semiconductor chip; placing said third semiconductor chip on said main surface of said second semiconductor chip in such a way that a back surface of said third semiconductor chip

interfaces with said main surface of said second semiconductor chip; electrically connecting said first semiconductor chip to said electrodes created on said wiring substrate through said protruding electrodes; and bonding said main surface of said first semiconductor chip to said main surface of said wiring substrate by a using an adhesive put between said main surfaces;

after said step of placing said first, second and third semiconductor chips on said wiring substrate, electrically connecting said electrodes created on said second semiconductor chip to said respective electrodes created on said wiring substrate by wires; and

after said step of placing said first, second and third semiconductor chips on said wiring substrate, electrically connecting said electrodes created on said third semiconductor chip to said respective electrodes created on said wiring substrate by wires,

wherein in said step of placing said first, second and third semiconductor chips on said wiring substrate, said third semiconductor chip is placed on said main surface of said second semiconductor chip in such a way that said electrodes created on said third semiconductor chip are positioned at locations on the outer side of an area in which said first semiconductor chip is placed but on the inner side of an area in which said second semiconductor chip is placed; and

wherein in said process to electrically connect said

electrodes created on said third semiconductor chip to said respective electrodes created on said wiring substrate, said wires are connected to said electrodes created on said third semiconductor chip with a portion of said adhesive placed between a plurality of electrodes provided on said third semiconductor chip, which are positioned at locations on an outer side of said first semiconductor chip, and said main surface of said wiring substrate in such a way that a gap between said back surface of said third semiconductor chip and said adhesive is smaller than the thickness of said third semiconductor chip.